GaAs MONOLITHIC SINGLE-CHIP TRANSCEIVER

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ABSTRACT

A single-chip transmiter/receiver MMIC operating from 1.25 to 3 Ghz and incorporating most of the RF functions of a modern communication system is presented. The device incorporates: a direct vector modulator with the neccesary phase shifter circuits, an output amplifier for the transmitter, a low-noise amplifier and a down-converter with image rejection. The circuit has 60 MESFET and more than 250 passive components in a 5.0 x 2.4 mm chip and has been manufactured using 0.5 micron GaAs MESFET process.

INTRODUCTION

The pressing need of reducing size and manufacturing cost of RF circuits motivated by the development of new mass production products as mobile or wireless systems, jointly with the recent advances in MMIC design, has conducted to the development of complete T/R subsystems integrated in a single-chip. In the last two years, several works have been presented describing devices with different functions and integration level.

The approach that we present has two important achievements: the use of direct I/Q modulation for the transmitter, and the reception with image-rejection. In addition to these features, the device has the advantadge of an ultra-wide operating band, allowing the use of the circuit in several mobile and fixed systems.

SYSTEM ARCHITECTURE

This device has been designed to be used in any type of digital radio-communication system operating in the range of 1.25 to 3 GHz. It can be applied to point-to-point or point-to-multipoint radio links, mobile and wireless communication systems. All these systems can operate in continuous or burst mode, and use any type of vector modulation as QPSK, 8PSK, 16QAM, 64QAM, etc. Digital frequency modulations as GMSK or FSK are also possible.

Transmitter has been designed to operate using direct modulation [1]. It works as an universal I/Q modulator, thus, it is not preset to a specific type of constellation. Any type of PSK or QAM modulation can be generated.

Baseband signals (I,Q) are applied to the chip with the coding of the chosen modulation, after proper filtering. The inputs of these signals are DC-coupled and have a bandwidth of more than 500 Mhz. Modulation is performed in linear mixers, generating a *clean* band-limited spectrum. This allows the control of the RF bandwidth at the base-band level, avoiding the need of expensive RF filters.

Receiver uses down-conversion to an Intermediate Frequency. This down-conversion is made with image rejection by using two mixers in 90° configuration [2]. Rx IF can be set at any value ranging from zero to 500 Mhz. Direct demodulation is also possible.

To simplify global system design, only one microwave oscillator is used to generate the transmission carrier frequency. The value of the IF is selected as the difference between Tx and Rx frequencies. This approach allows to share for Tx and Rx the phase shifter circuit located inside the chip.

To build a complete RF transceiver, only the LO and the power amplifier need to be added. An additional LNA first-stage can be optionally added if a better receiver sensitivity is required.

CIRCUIT DESIGN

The block diagram of the circuit is presented in figure 1. The device incorporates:

-A direct-vector modulator, composed of a 90° broadband phase-shifter, two couples of differential amplifiers, two active double-balanced mixers, a differential amplifier, and an active balun stage.

-A two-stage amplifier for the Transmitter output.

-A Low Noise Amplifier as receiver input.

-An Image Rejection Down Converter composed by a driver stage and two double-balanced mixers. This Image Rejection Mixer shares with the modulation section the 90° phase-shifter.

A. 90° Phase-Shifter.

The 90° broadband Phase-Shifter is based on two 2nd order RC networks that are used combined with differential amplifiers.

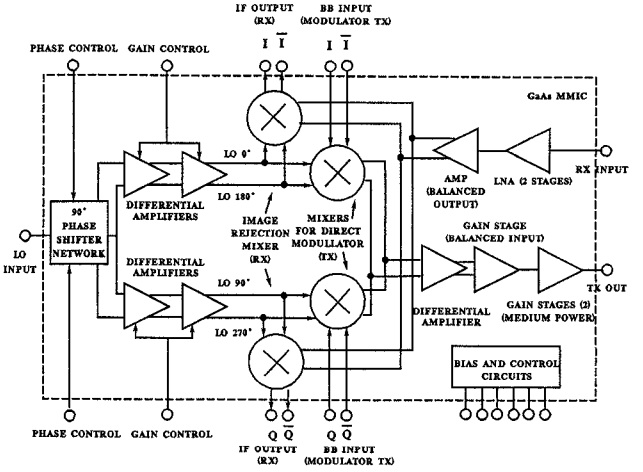

Fig.1. Block diagram of the circuit.

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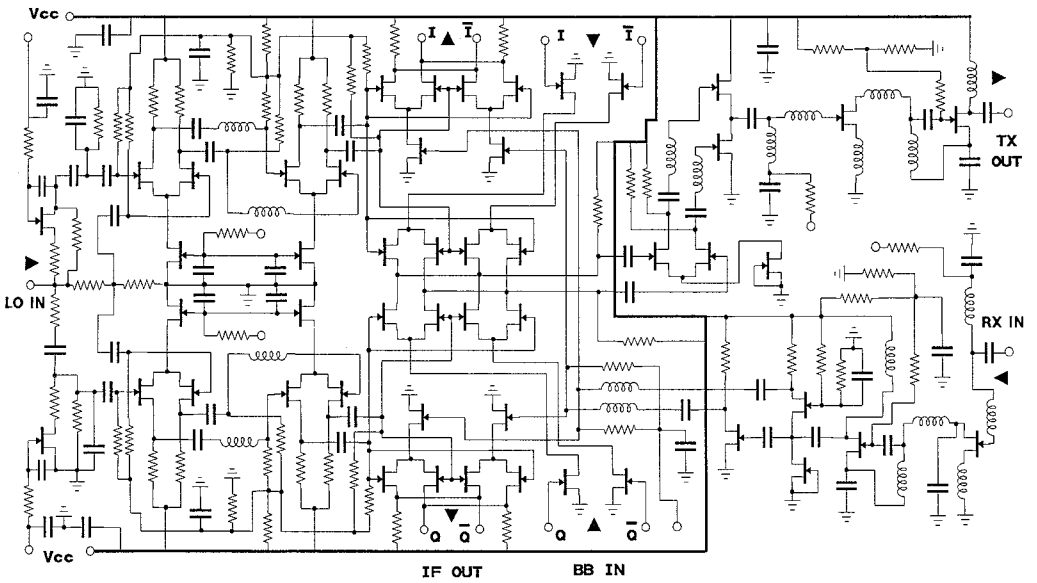

Fig.2. Electric Schematic of the circuit.

The basic structure is shown in fig. 3. This circuit supplies over the whole bandwidth (1.25- 3 Ghz) four signals delayed 0, 90, 180 and 270 degrees, with very small phase and amplitude errors. Real measurements demonstrate a phase error less than 1° and an amplitude error less than 0.3 dB. This structure and its design equations are described in detail in [4]. Its design is based on the work previously reported in [3].

Regarding to [4], the following changes have been performed: 1) sizes of the devices used in the differential amplifiers have been increased in order to rise the gain and compensate that they have now to drive more mixers, 2) inductive matching networks have been introduced to improve the operation in the upper part of the operating band 3) components of the RC branches have been recalculated according to the new bandwidth and the different sizes of the devices. With these improvements the necessary LO level may be reduced in about 8 dB, despite that the phase shifter has now to drive twice the load.

The phase fine-trimming system included in [4], based in *cold* FETs, is also used here.

B. Modulator.

Mixer stages of the transmitter are active four-quadrant multipliers based on the Gilbert Cell [5]. The circuit uses two identical mixing cells for the In-phase and Quadrature channels. All devices of the cell operate with non-saturated signal levels, generating an output signal that is proportional to the levels of both: base-band and LO inputs. Baseband inputs are balanced and DC-coupled allowing a maximum modulating frequency in excess of 500 Mhz.

The modulator can also be used as a Singe-Sideband Up-Converter if the system uses Tx IF.

The outputs of the I and Q channel mixers are added in balanced mode by the combination of the drain currents of the transistors. A differential amplifier is used to subtract these signals and eliminate traces of common-mode carrier and spurious signals. A *balun* stage composed of a source-follower and a common-source devices, transform the balanced output to a single-ended signal.

Inductive matching networks have been introduced to improve the response at the higher frequencies.

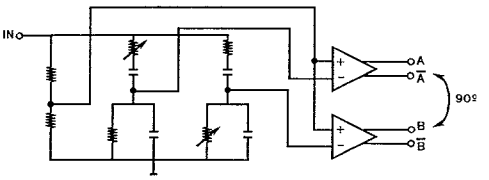

Fig.3. Basic diagram of the 90° phase shifter.

C. Output Amplifier

A two stage common-source amplifier is used as output stage of the transmitter. This amplifier uses a 900 μm width transistor as last stage and allows a maximum output level of 14 dBm (1 dB compression point). In normal operation of the modulator, it works below its compression point in the range of -5 to +5 dBm output level.

In order to save power, these two last stages are serially-biased by the same current.

D. Low Noise Amplifier (Receiver)

The LNA is a two stage circuit with reactive match. The first stage uses reactive serial feedback in the FET source, allowing simultaneous noise and impedance matching [6].

The LNA has a gain of 18 dB, a noise figure of 1.8 dB and an input S11 better than -13 dB over the whole bandwidth (1.25-3 Ghz).

E. Image Rejection Mixer

This circuit includes an Image Rejection Mixer, based on two mixers operating in quadrature, to avoid the need of external passive filters [2].

The RF signal (output of the LNA) is split in two balanced components by an amplifier stage, composed by a common-gate/common source-couple of transistors. This pair of balanced signals is additionally split in-phase, and each component is sent in balanced mode to the two mixers.

The Local-Oscillator 90° phase shifter and its differential amplifiers are shared with the transmitter section.

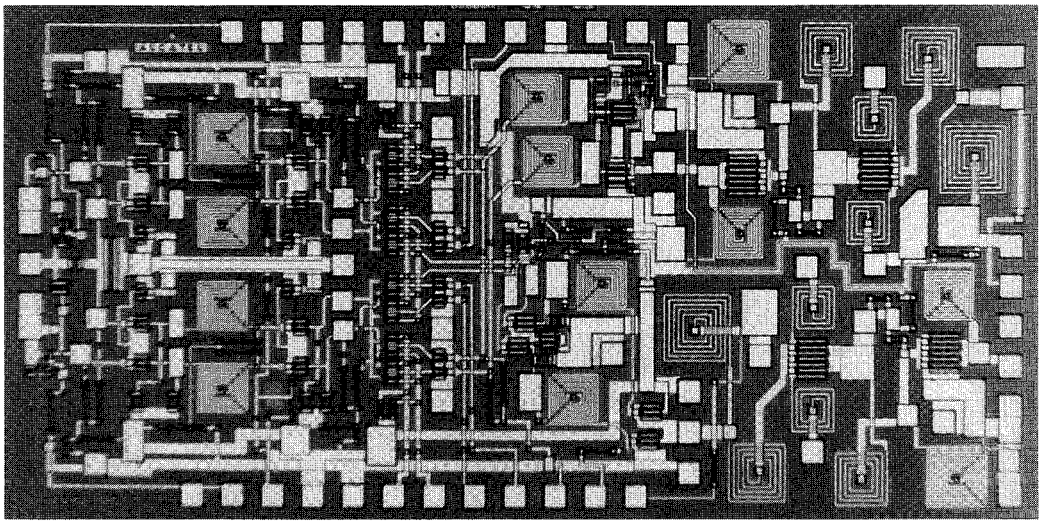

Fig.4. Chip photograph.

The mixers employed for the Image-Rejection Mixer are Gilbert-cell double-balanced mixers, similar to those included in the modulator. These cells operate with balanced signals.

The IF output of both mixers is extracted out of the chip from the drains of the Gilbert cells in balanced mode with an output impedance of 400 Ω. These balanced signals must be externally converted to single-ended (using a differential amplifier or a passive balun) and introduced in a 90° coupler to obtain the desired IF side-band. We have preferred not to spend GaAs area to implement low-frequency circuits by cost and performance reasons (flicker noise).

As the IF outputs are DC-coupled, the Intermediate Frequency can be set at any value ranging from zero (direct-demodulation) to more than 500 Mhz.

Due to the high impedance level of the IF outputs, it is advisable to use external IF driving circuits at the output of the circuit. (See fig.5)

A simple solution is to place a small-signal npn transistor operating as emitter-follower at each IF output. The 180° and 90° couplers are passive, as shown in fig. 5. With this solution, overall receiver conversion gain is about 20 dB.

A second approach is to use a 180° balun with impedance transformation ratio. The theoretical conversion gain is in this case 12 dB.

IF outputs can be directly connected (unmatched) to a 50 Ω coupler. However, the conversion gain drops to 5 dB.

Measurements presented in figs. 9 and 10 have been made on this configuration.

The most interesting solution, is to use a silicon monolithic differential amplifier, with high input impedance, avoiding the use of passive 180° baluns. In this case, assuming that the amplifier could drive a 50 Ω output load, Rx Conversion Gain would be approximately 20 dB plus the voltage gain of the amplifier.

F. Bias, Layout and Fabrication

There is only one positive supply voltage with consumption. Several positive reference voltages are obtained from this source. To avoid any undesired coupling between different sub-circuits by the power wires, there are more than 80 pF of capacitors inside the chip between the power and ground. The negative bias are supplied by six different pads. There is no power consumption from these voltage:

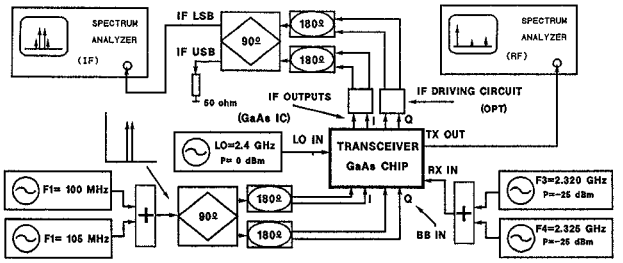

Fig.5. Test setup used to obtain measurements shown in Fig.8 and Fig.9.

This allows to separately bias the different sections of the circuit, to simplify dc-testing of the device.

By applying the pinch-voltage to these pads, it is possible to turn off different sections or the whole circuit. This is useful in burst transmitters, or if not all the circuit functions are been used.

The device has been designed to be fully on-wafer testable using coplanar high frequency probes.

A complete schematic of the circuit is presented in fig. 2.

Chip size is 5.0 x 2.4 mm and total power consumption is 180 mA at 6.5 volts. Power consumption when only Tx and Rx are operating are 140 and 120 mA respectively. A photograph of the chip is shown in figure 4.

Linear and non linear simulation software were used in circuit design. Active devices were modeled using the Curtice cubic model [8].

The circuit has been manufactured by GEC-Marconi using the process F20. Manufacturing process includes D-type 0.5 μm MESFET, two metal levels, and via-holes.

MEASUREMENTS

Figures 6 to 10 show different measurements of the circuit. To test the modulator, we have used a vector network analyzer. Phase and amplitude errors of the constellation vectors were measured applying the different symbols at slow data rate. Figure 6 shows a QPSK constellation. Fig. 8 shows the transmitter output spectrum generated by using the test set-up of figure 5. LO level was 0 dBm. With this assembly, the output spectrum should be an SSB

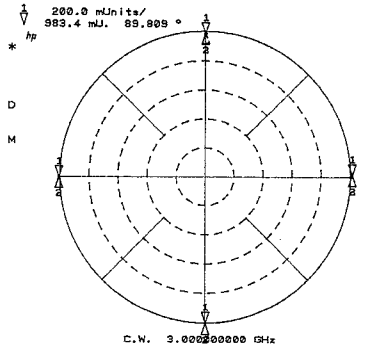

Fig.6. QPSK modulation.

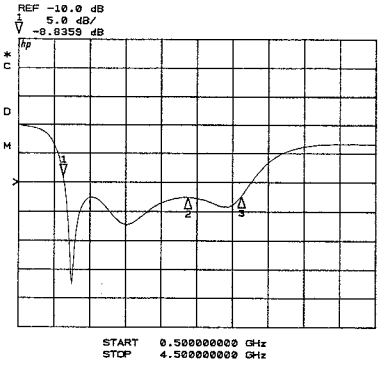

Fig.7. Input matching at LNA port.

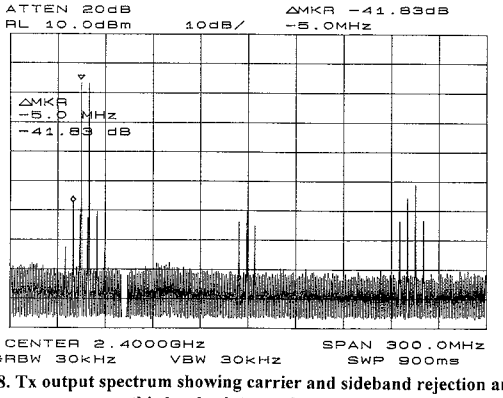

Fig.8. Tx output spectrum showing carrier and sideband rejection and third order intermodulation.

modulation. This figure allows to appreciate carrier and sideband suppression, and third order intermodulation levels. Modulator phase and amplitude errors can be extracted from these measurements [1], [4].

Input match at the LNA port is shown in figure 7.

Figure 9. shows an intermodulation test at Rx with the setup shown in fig.5.

The Image Rejection is demonstrated in figure 10. In this measurement, output level versus IF frequency for the signal and image sidebands can be appreciated. To make these measurements, we applied to the Rx input of the device a tone that was swept from 2.2 to 2.6 Ghz. IF circuits were as fig. 5, and the connection of the 90° coupler was done to select the lower side-band. IF 90° coupler center frequency was 100 Mhz. LO was fixed at 2.4 Ghz and spectrum analyzer was configured to trace the peak level. The high-level line is traced when the RF input is swept from 2.2 to 2.4 GHz, and low-level line when it is swept from 2.4 to 2.6 GHz. Image

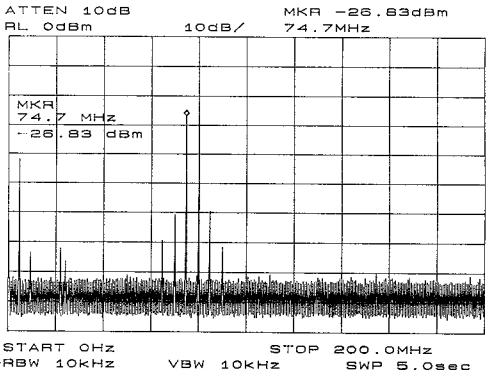

Fig.9. Receiver output spectrum at IF port showing two tone intermodulation.

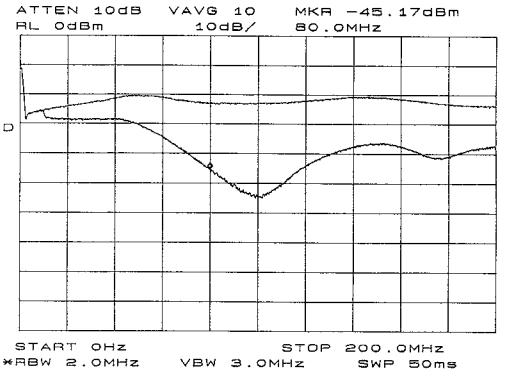

Fig.10. Image rejection test. Receiver IF output spectrum with LO=2.4 Ghz, sweeping an RF tone from 2.2 to 2.6 GHz.

rejection is about 25 dB. It can also be appreciated that conversion gain is mainly independent of the chosen IF frequency.

Measurements shown in figs.9 and 10 have been made without any IF driving circuit, connecting directly the 400 Ω IF outputs to the 50 Ω ports of the passive couplers. This must be taken into account to calculate the conversion gain.

CONCLUSIONS

A single-chip including most of the RF circuits required by a microwave transceiver has been presented. The device includes: a complete direct vector modulator, a medium power output amplifier, a low-noise amplifier and an image rejection down-converter. The wide radiofrequency (1.25- 3 GHz), base-band and IF bandwidth (DC to 500 MHz) allows the use of the device in a broad range of communication systems, including mobile and wireless systems, and high capacity terrestrial or satellite radio links.

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